In the Claims:

Kindly rewrite the claims to read as follows:

1. (Currently Amended) A method for producing integrable semiconductor components, in particular transistors, diodes, and logic gates, starting with a p-doped or n-doped semiconductor substrate in the following steps:

application of a mask onto the semiconductor substrate for definition of a window delimited by a peripheral edge;

production of an n-doped trough in the p-doped semiconductor substrate or p-doped trough in the n-doped semiconductor substrate by means of ion implantation through the mask using ~~an~~ a high energy that assures that a p-doped inner area remains on a surface of the p-doped semiconductor substrate or an n-doped inner area remains on a surface of the n-doped semiconductor substrate, ~~whereby~~ the p-doped or n-doped inner area having a same doping concentration as the starting semiconductor substrate, wherein a fringe area of the n-doped trough or p-doped trough extends up to the surface of the semiconductor substrate; and

production of additional n-doped and/or p-doped areas in the p-doped or n-doped inner area and in the fringe area of the n-doped or the p-doped trough that form the structure of the semiconductor component without a step of additional doping of the p-doped inner area or n-doped inner area to prevent turnover of conductivity type.

2. (Previously presented) The method of Claim 1 wherein, for creation of the structure forming an NPN-transistor, a p-doped area having heavier doping than that of the semiconductor substrate together with the p-doped area enclosed by the p-doped inner area forming the base of the transistor and an n-doped area forming the emitter of the transistor are produced in the p-doped inner area, whereby the n-doped trough forms the collector of the transistor.

3. (Previously presented) The method of Claim 2, wherein the n-doped area forming the emitter has heavier doping than that of the n-doped trough.

4. (Previously presented) The method of claim 2, wherein an n-doped junction area having heavier doping than that of the trough is produced in the n-doped fringe area of the trough and a p-doped area having heavier doping than that of the p-doped area enclosed by the p-doped inner area is produced in the p-doped area enclosed by the p-doped inner area.

5. (Previously presented) The method of Claim 1, wherein for the creation of a structure forming a PNP-transistor an n-doped area enclosed by the p-doped inner area is produced in the p-doped inner area and forms the base of the transistor and in the n-doped area a p-doped area forming the emitter of the transistor is produced, whereby the p-doped inner area forms the collector of the transistor.

6. (Previously presented) The method of Claim 5, wherein the p-doped area forming the emitter of the transistor has heavier doping than that of the semiconductor substrate.

7. (Previously presented) The method of Claim 5, wherein in the n-doped fringe area of the trough an n-doped area having heavier doping than that of the trough and in the n-doped area forming the base an n-doped area having heavier doping than that of the n-doped area forming the base and in the p-doped inner area a p-doped area having heavier doping than that of the p-doped inner area are produced.

8. (Previously presented) The method of Claim 1, wherein for the creation of the structure forming an NPN-transistor having high gain in the p-doped inner area an n-doped area forming the emitter of the transistor is produced, whereby the p-doped inner area forms the base and the n-doped trough forms the collector of the transistor.

9. (Previously presented) The method of Claim 8, wherein an n-doped area having heavier doping than that of the trough and in the n-doped area forming the emitter an n-doped area having heavier doping than that of the area forming the emitter and in the p-doped inner

area a p-doped area having heavier doping than that of the p-doped inner area are produced in the fringe area of the n-doped trough.

10. (Previously presented) The method of Claim 1, wherein an n-doped area joining the fringe area of the n-doped trough with the p-doped inner area and in the p-doped inner area at least one n-doped area are produced for the creation of the structure forming an I^2L element, whereby the p-doped inner area forms the base of a multi-collector transistor and at least one n-doped area enclosed by the p-doped inner area forms the individual collectors of the transistor.

11. (Previously presented) The method of Claim 10, wherein in the n-doped area joining the fringe area of the n-doped trough with the p-doped inner area a p-doped area is inserted.

12. (Previously presented) The method of Claim 11, wherein a p-doped area having heavier doping than that of the semiconductor substrate and in the at least one n-doped area enclosed by the p-doped inner area an n-doped area having heavier doping than that of the n-doped area are produced in the p-doped inner area.

13. (Previously presented) The method of Claim 1, wherein for the creation of a structure forming a field effect transistor an n-doped area forming the gate of the transistor is formed in the p-doped inner area, which partitions the p-doped inner area into two regions one of said regions forming the drain and the other region forming the source of the transistor.

14. (Previously presented) The method of Claim 13, wherein a p-doped area having heavier doping than that of the p-doped inner area is inserted in the regions of the p-doped inner area forming the drain and the source, respectively.

15. (Previously presented) The method of Claim 13, wherein an n-doped area having heavier doping than that of the n-doped area forming the gate is inserted into the n-doped area forming the gate.

16. (Previously presented) The method of Claim 1, wherein an n-doped area enclosing each active area is produced in the semiconductor substrate for the purpose of separation of active areas for individual semiconductor components.

17. (Previously presented) The method of Claim 16, wherein the n-doped area enclosing the active area extends up to the n-doped trough of the semiconductor substrate.

18. (Previously presented) The method of Claim 1, wherein for the separation of active areas for individual semiconductor components in the semiconductor substrate prior to ion implantation a mask enclosing each active area is applied to the semiconductor substrate and after application of the mask the n-doped trough is produced in the semiconductor substrate by means of ion implantation, such that the trough is pulled up in the area underlying the mask.

19. (Previously presented) The method of Claim 18, wherein an n-doped area that extends up to the raised area of the n-doped trough is produced in the semiconductor substrate.

20. (Previously presented) The method of Claim 18, wherein an oxide layer in the semiconductor substrate produces an area of the n-doped trough reaching upward to beneath the oxide.

21. (Previously presented) The method of Claim 1, wherein active areas for the individual semiconductor components are separated in the semiconductor substrate by trenches.

22. (Previously presented) The method of Claim 16, wherein n-doped or p-doped areas for the creation of the structures forming the semiconductor components are produced in the active areas.

23. (Previously presented) The method of Claim 1, wherein for the creation of the structure forming a photosensitive diode at the fringe area of the n-doped trough an initial terminal is created and at the p-doped inner area a second terminal is created.

24. (Previously presented) The method of Claim 1, wherein for the creation of the structure forming a photosensitive diode in the semiconductor substrate outside of the n-doped trough a p-doped area is implanted, whereby the first terminal is created at the p-doped area implanted into the semiconductor substrate and the second terminal is created at the fringe area of the n-doped trough.

25. (Previously presented) The method of Claim 1 employed for the creation of a structure forming a photosensitive transistor in which an n-doped area is implanted into the p-doped inner area, whereby the terminal forming the collector at the fringe area of the n-doped trough and the terminal forming the emitter at the n-doped area implanted into the p-doped inner area is created.

26. (Previously presented) The method of Claim 1, wherein the p-doped or the n-doped semiconductor substrate is a weakly p-doped or n-doped semiconductor substrate.

27. (Previously presented) The method of Claim 1, wherein for the creation of a lateral transistor in the n-doped trough or p-doped trough of the semiconductor substrate an n-doped or p-doped trough forming a second diactive base of the transistor is produced by means of ion implantation.

28. (Deleted)

29. (Previously presented) The method of claim 1 wherein the energy of said ion implantation is about 6 MeV.

30. (Previously presented) The method of claim 1 wherein the ion implantation energy is 6 MeV phosphorous ions at a dose of 2×10^{13} atoms/cm^2.

31. (Currently amended) The method of claim ~~28~~ 1, wherein the starting semiconductor substrate has a low doping concentration (p-) or (n-).